Digital Applications and Education with SFL and FPGA

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Agenda

Education/Research Projects with SFL at Shimizu Laboratory in Last Y

- Undergraduate Project Example -- Video Game
- Undergraduate Project Example -- PDP11 Compatible CPU
- Undergraduate/Master Project Example -- USB Device Contoler
- Research Project Example -- MP3 Hardware Encoder
- Research Project Example -- USB 2.0 High Speed Controler
- Research Project Example -- Java Processor
- Research Project Example -- Latency Tolerant Processor

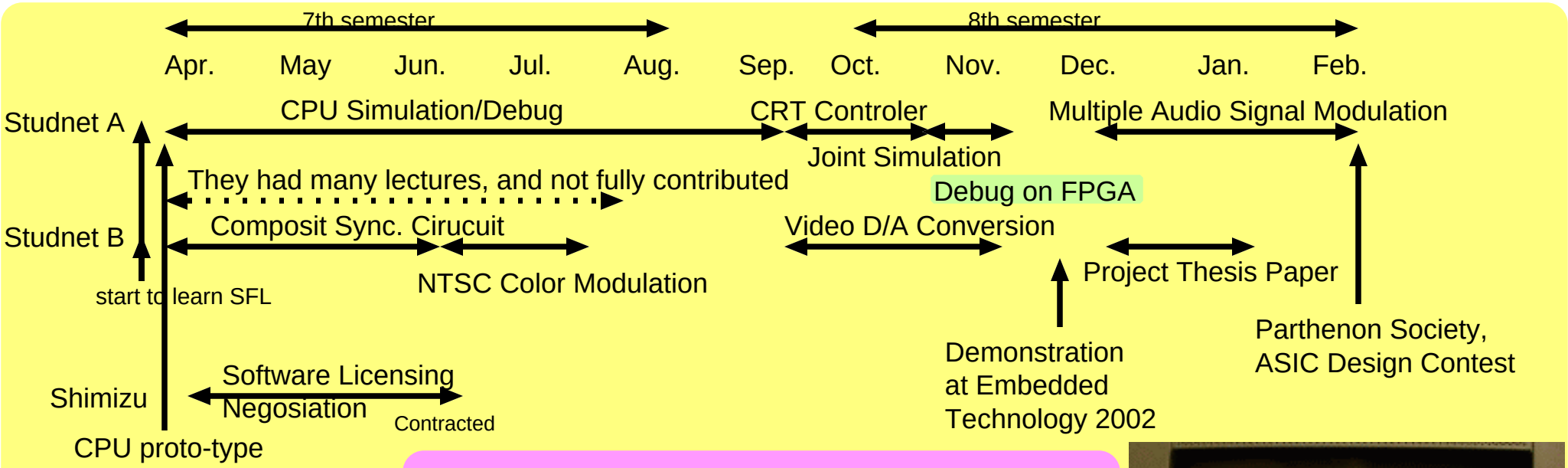
Last year, I have no doctorial students, no research assistant, 5 master students, 8 undergraduates.
All of these projects are carried out with 3 master and 4 undergraduates.

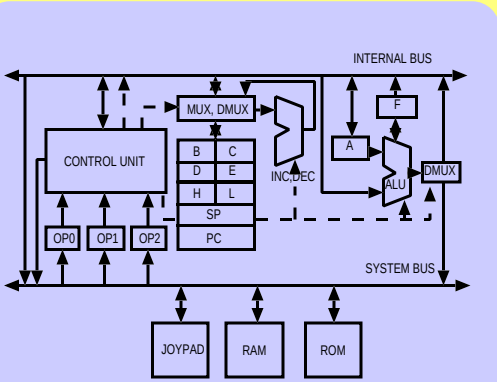
Undergraduate Curriculum for Microelectronics in our department

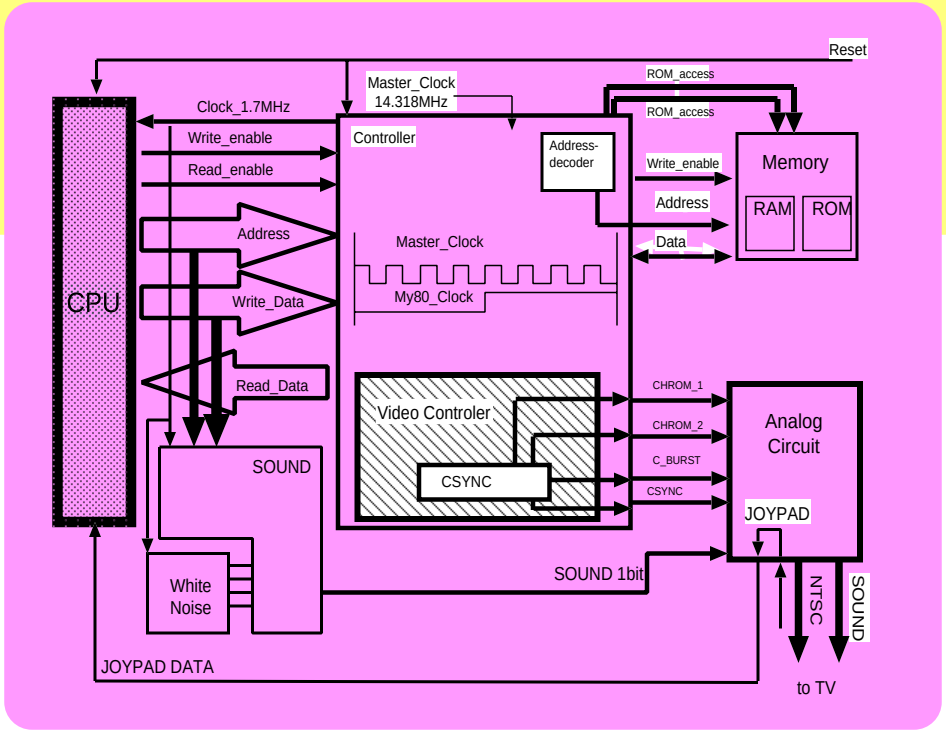
Demonstration of SFL development environment

Conclusion

Undergraduate Project Example -- Video Game







Device name	EPF10K30E-3
logic elements	1503
Max Freq.	20MHz

Undergraduate Project Example -- PDP11 Compatible CPU

7th semester — 8th semester

Apr. May Jun. Jul. Aug. Sep. Oct. Nov. Dec. Jan. Feb.

Studnet C

CPU Specification/Logic/Simulation

GCC/RTOS poring

MMU/UNIX

POP-11/10 for Embedded

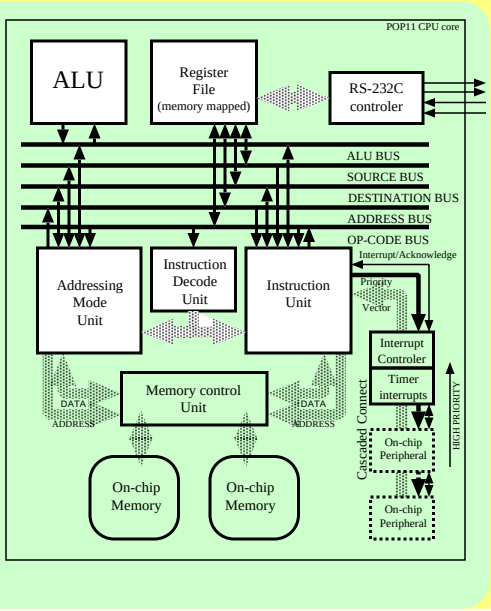
Debug on FPGA

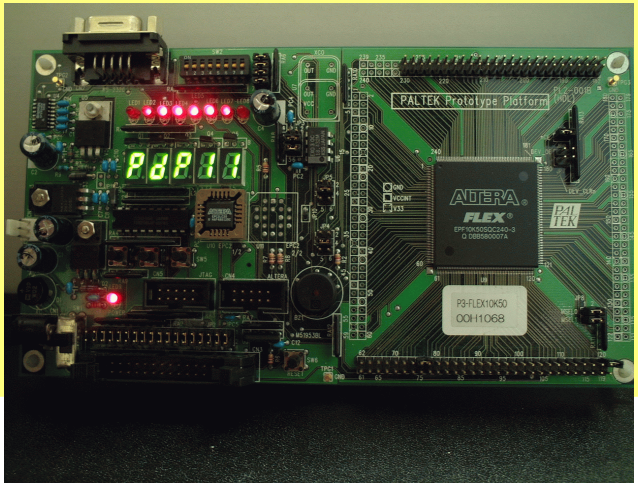
POP-11/40*

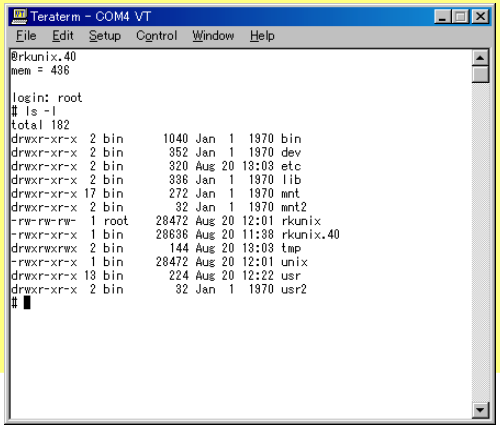
Parthenon Society, ASIC Design Contest

Demonstration at Embedded Technology 2002

UNIX V6 boot and working







CPU	Logic Cells	Max Freq.	FPGA
POP-11/10	1678 LCs	9 MHz	EPF10K30EQC208-3
POP-11/40*	2687 LCs	20 MHz	EP1K100QC208-1

Undergraduate/Master Project Example -- USB Device Contoler

Dec. Jan. Feb. Mar. Apr. May Jun. Jul. Aug. Sep. Oct. Nov.

Master A — USB specification/IF logic

Studnet D — USB spec./MPU Firmware → USB specification/IF logic

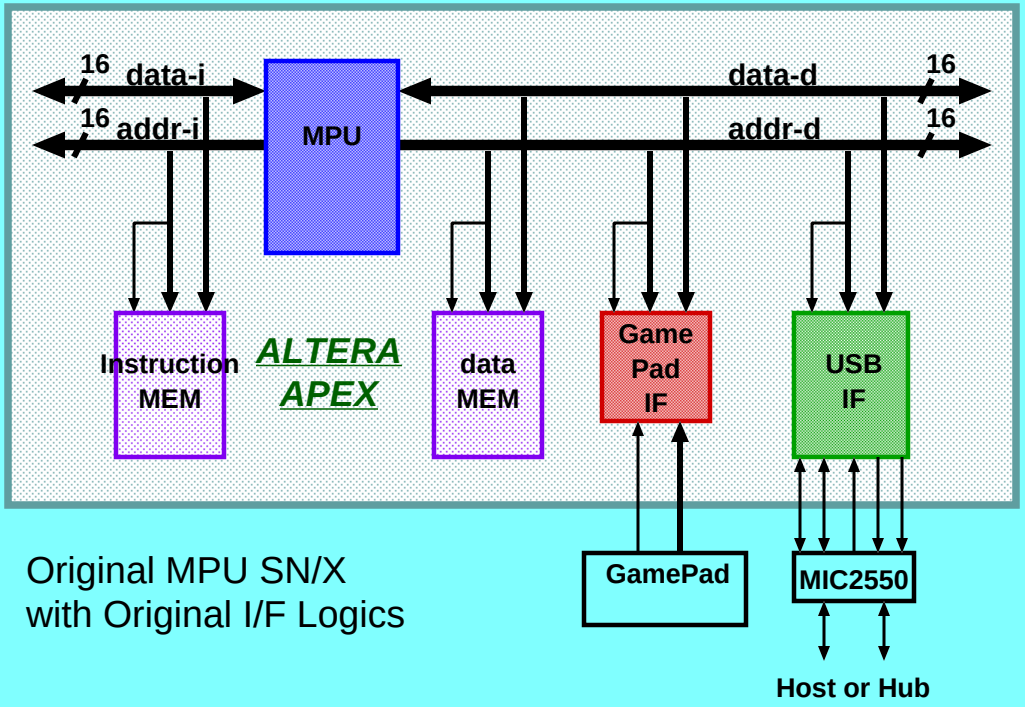
Debug on FPGA

USB 2.0 Project started

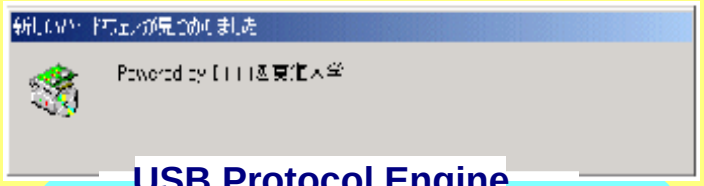
Parthenon Society,
ASIC Design Contest

Demonstration
at Embedded
Technology 2002

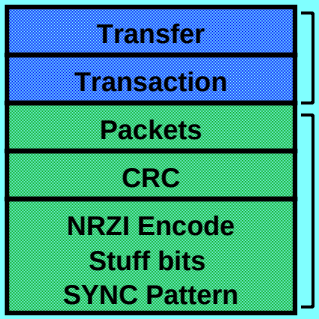
Modules



Original MPU SN/X
with Original I/F Logics



USB Protocol Engine

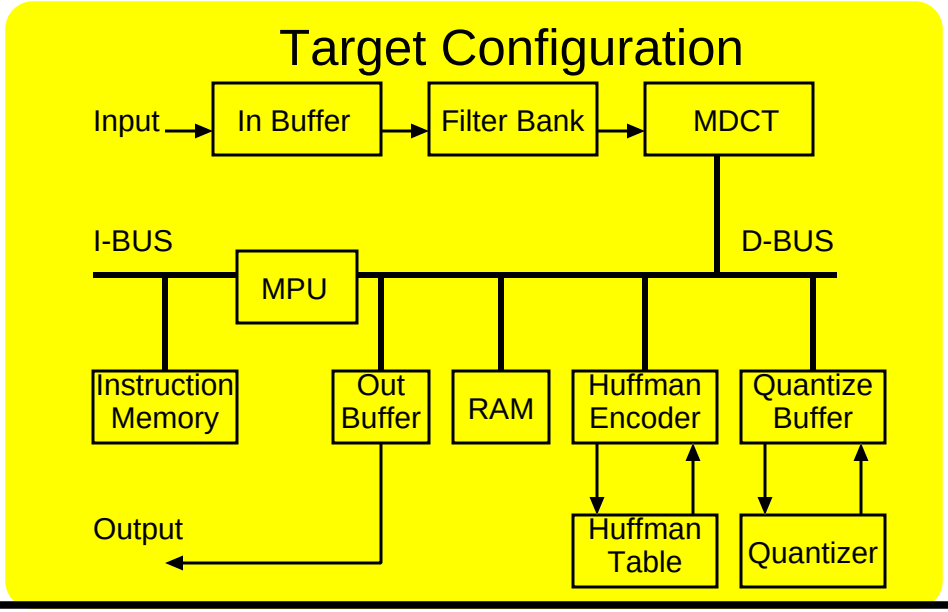


Device name	EP20K1000CF672C7
total logic elements	1617
Max Freq.	52.52MHz

Research Project Example -- MP3 Hardware Encoder

With new hardware algorith,
we will build a high speed,
low power MP3 encoder LSI.

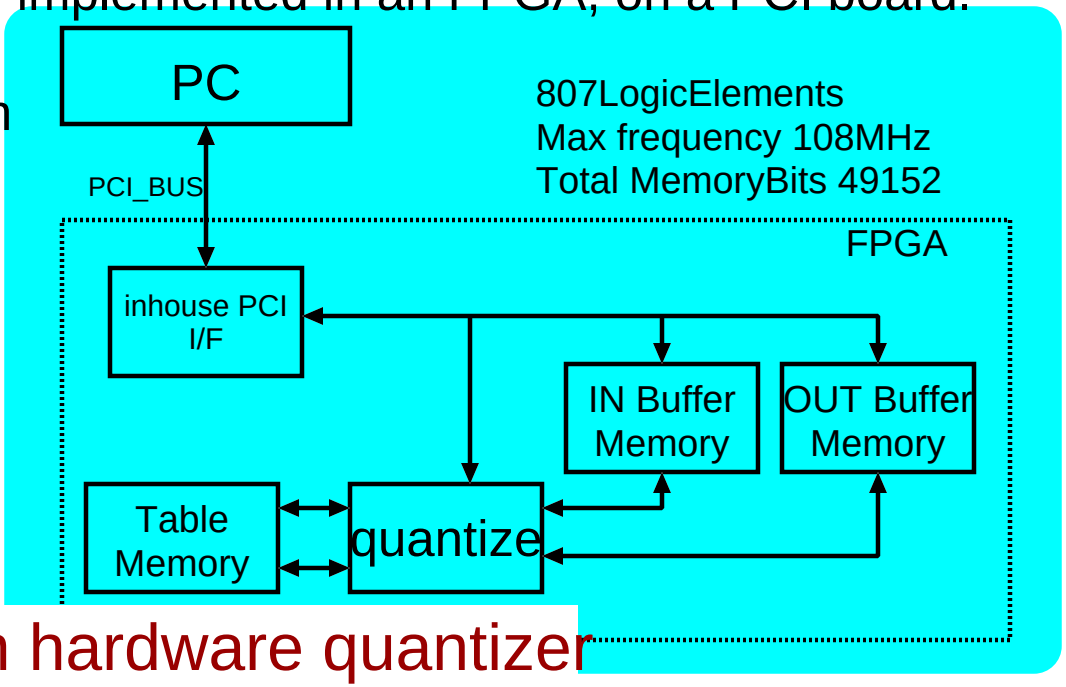
We are implementing all of the
features within an FPGA.



Current Status: demonstrate quantizer implemented in an FPGA, on a PCI board.

MP3 Encoder Performance Comparison
to encode a music song on a PC.

	Software	with quantize logic
real	44m59s	9m59s
user	43m22s	6m39s
sys	0m03s	2m59s



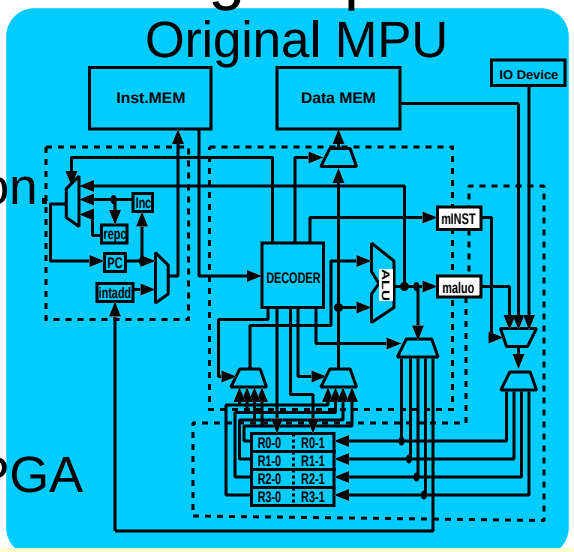
4 times speedup achieved with hardware quantizer

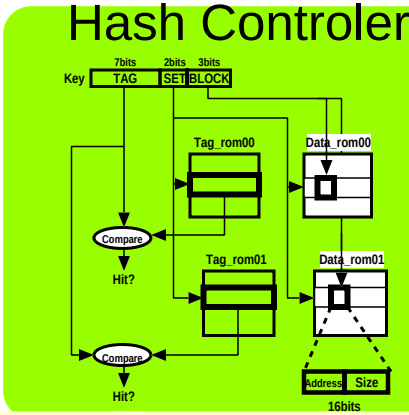
Research Project Example -- USB 2.0 High Speed Controler

Designing High Speed USB 2.0 Controler
with Hash controler for packet descrimination

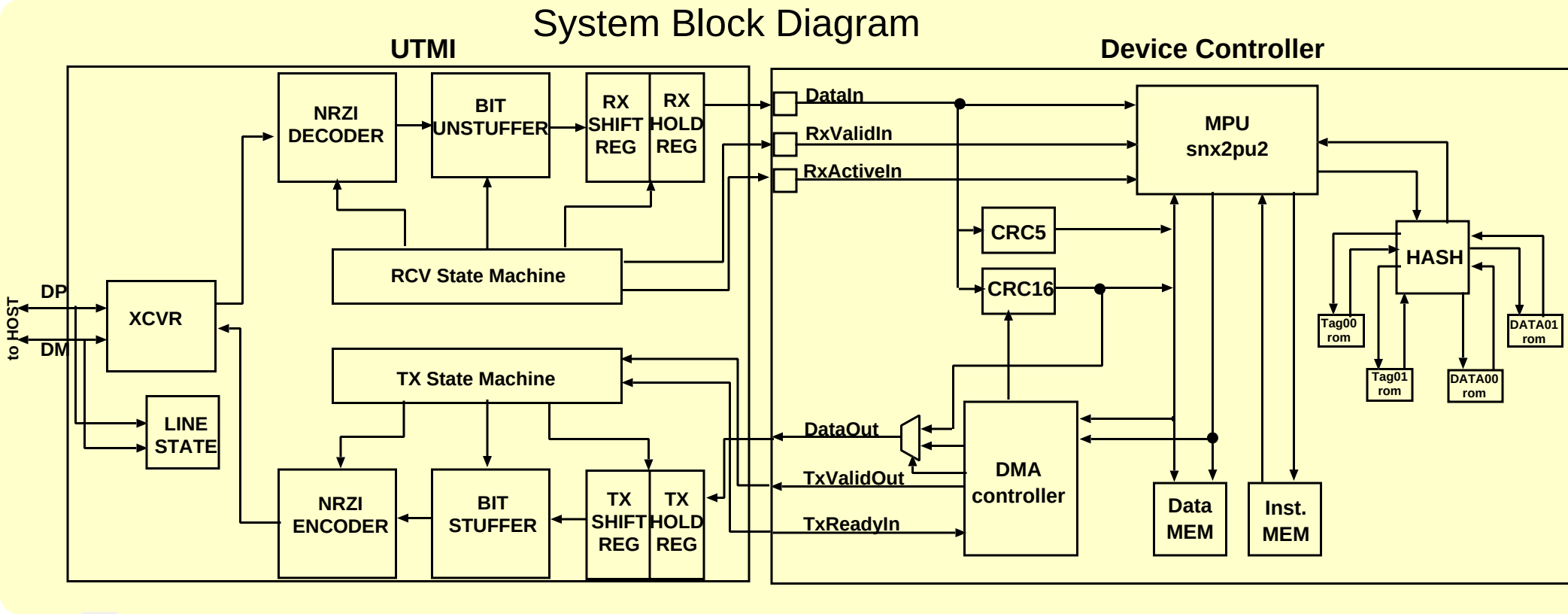
UTMI controler for USB1.1 is inhouse.
UTMI for USB 2.0 is in market.

Current Status: Begining to debug on an FPGA





System Block Diagram



Research Project Example -- Java Processor

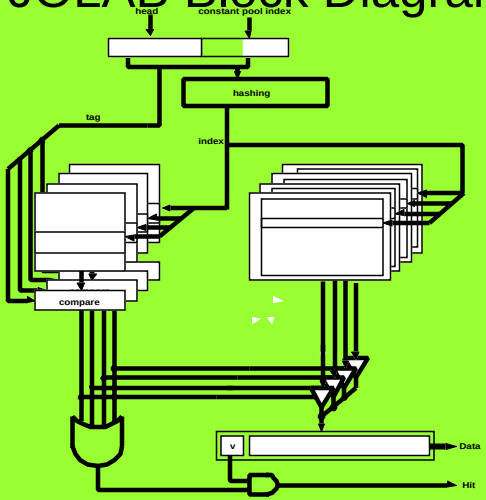
TRAJA Processor: Queued Pipilining Java Processor

Designing state of art Java processor

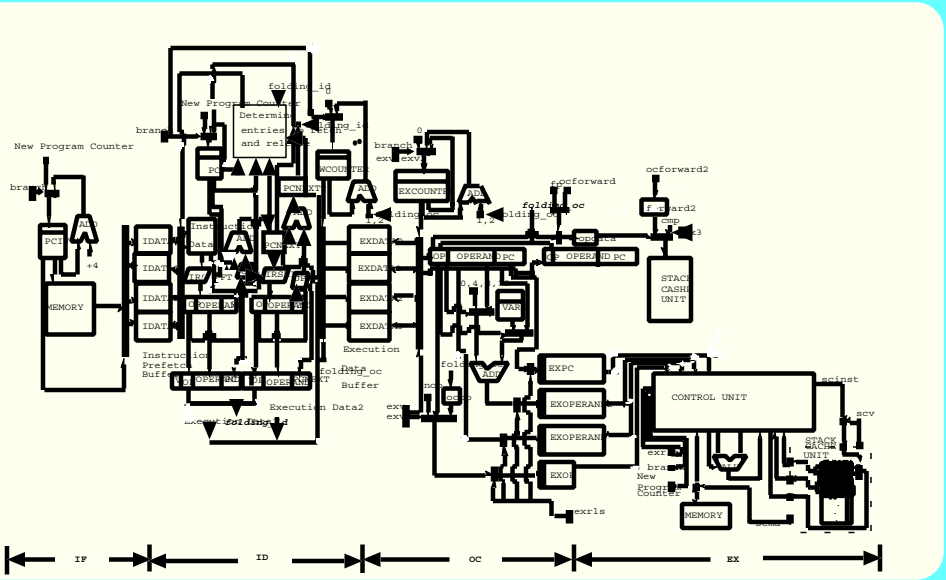
JOLAB: Java Object Look Aside Buffer

Reduce Resolution Overhead for Embedded Applications
It is also working for software JVM.

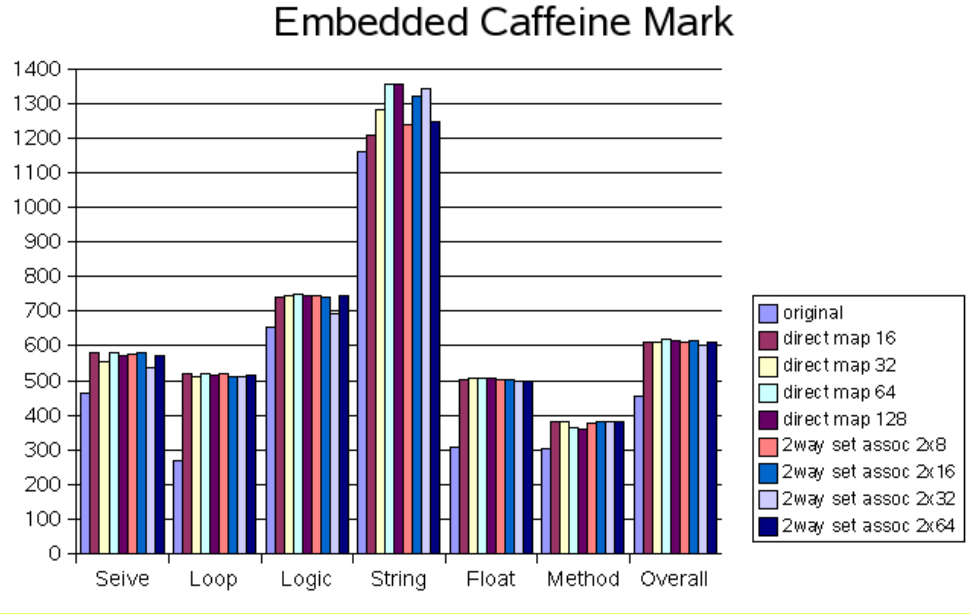
JOLAB Block Diagram



TRAJA Block Diagram



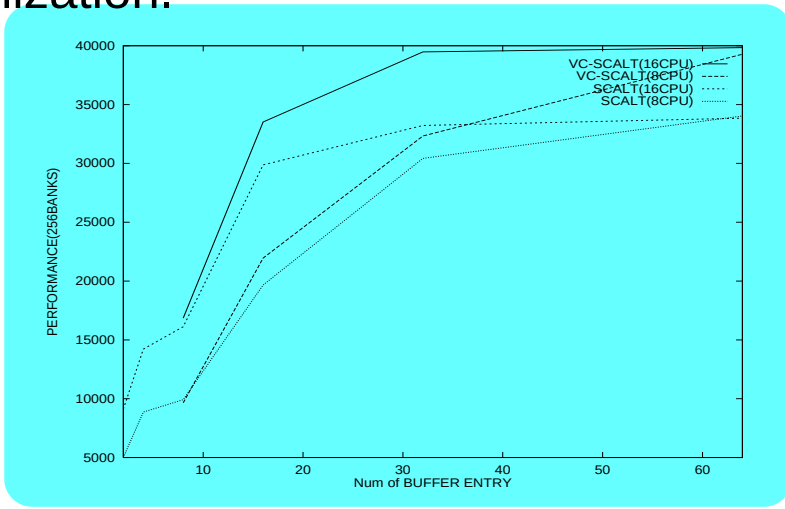
JOLAB Benchmark based on Kaffe



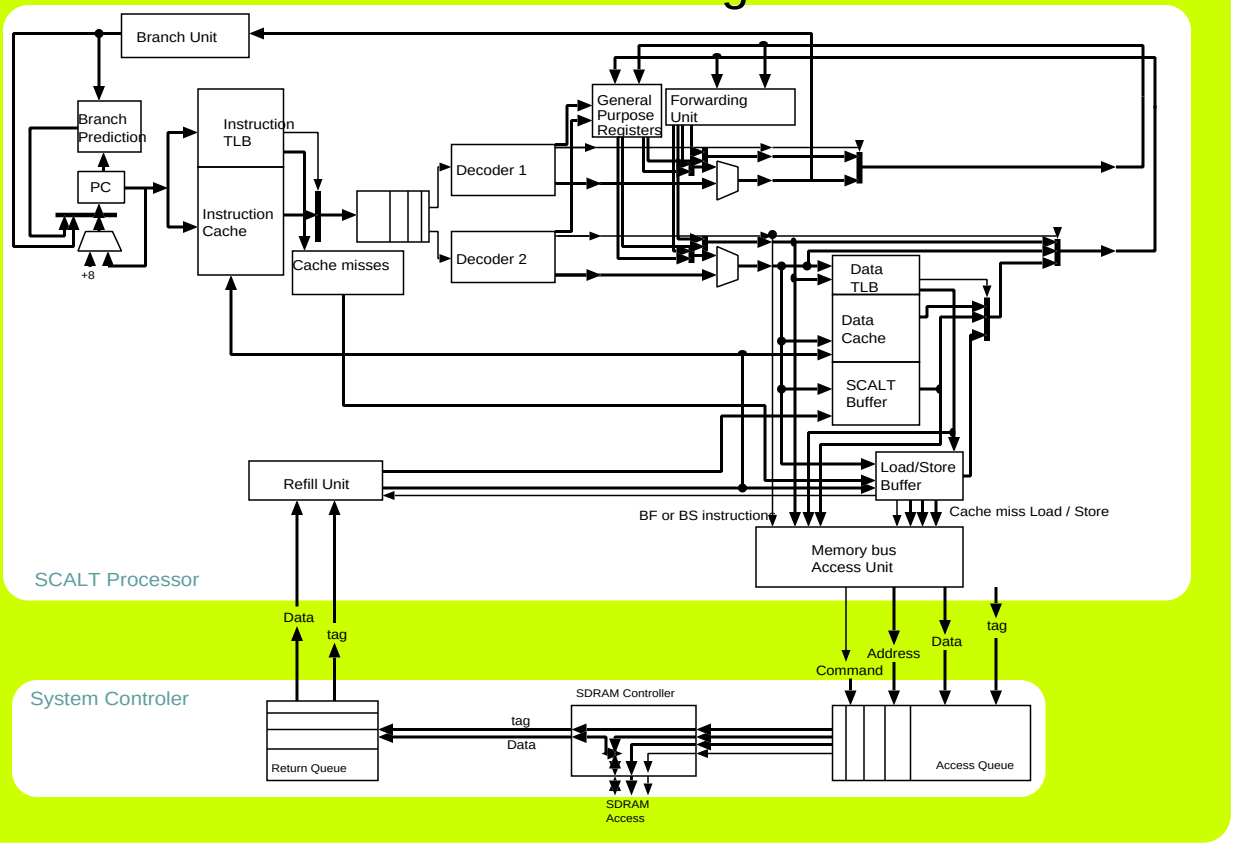
Research Project Example -- Latency Tolerant Processor

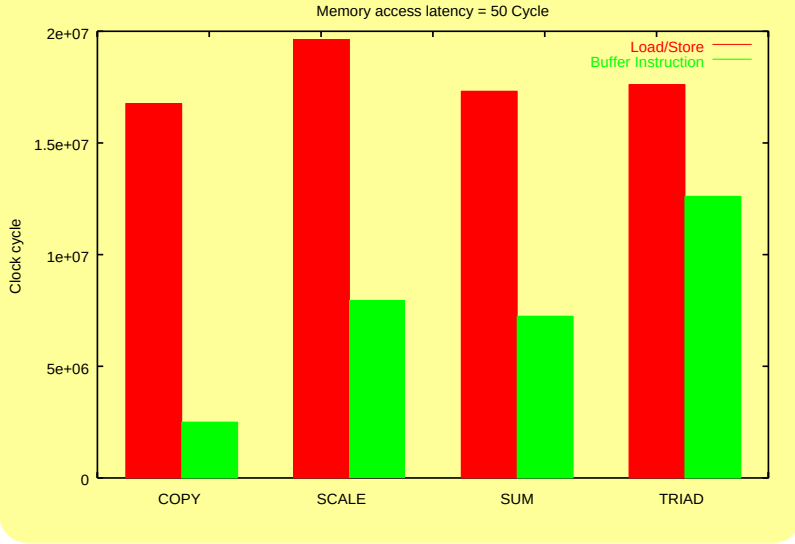
Scalable Latency Tolerant Processor (SCALT) Project

Dual Issue Alpha Compatible Instruction set with SCALT extensions.
High performance processor with simple organization.



SCALT Block Diagram





Undergraduate Microelectronics Education at Tokai University

Semester	Lectures (credit)
1-4	Pulse Circuit(4), Digital Circuit(4)
5	Computer Engineering(4), Integrated Circut Engineering(4)
6	Computer Systems(4), VLSI Design Seminar I(2)
7	VLSI Design Seminar II(2)
8	none

Join to Lab.

CMOS circuit, Schematic Diagrams

Spice Simulation and LSI Layout with Magic

CPU Design with SFL

Demonstration

Conclusion

SFL benefit for research/education in ASEAN

Fast Startup of Students

Most undergraduate students start to design original processor within 2 months

Cost Effective

PARTHENON Society can provide access to CAD system.
FPGA vendors provide web version of FPGA fitter/placer.

Competitive Design Language for VLSI

We can take different approach than US or EU.

With SFL, I had designed 6502 compatible MPU within 2 days.
Four people at NTT designed DLX compatible MPU in 4 days.
At this time, C based design is far from practical.

SFL benefit for startup companies in ASEAN

Same as above, and we sould not pay to much money on tools!

I believe that the microelectronics activity in ASEAN will lead 21st Century.

There is no silver bullet, but most US engineers only started with Mead and Conway(1980).
It is only 20 years experience. We will be able to beat them with strategic alliance in ASEAN.